WHAT IS CLAIMED IS:

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 A semiconductor integrated circuit, comprising:

a current generator circuit that generates a first current substantially proportional to an absolute temperature, the first current being determined by a size ratio of a MOS transistor, and by a resistor; and

a starting-up circuit that causes said current generator circuit to generate the first current at a stable working point of said current generator circuit,

wherein

while said current generator circuit operates at the stable working point, a current that flows through said starting-up circuit is determined by a diffusion resistance and a MOS transistor connected in series.

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2. The semiconductor integrated circuit as claimed in claim 1, further comprising:

a voltage generator circuit that generates

30 a reference voltage substantially independent of the
absolute temperature using the first current
generated by said current generator circuit.

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3. The semiconductor integrated circuit as

claimed in claim 2,

wherein

said voltage generator circuit comprises: one of a bipolar transistor and a diode;

5 and

a resistor connected to said bipolar transistor or said diode; and

said voltage generator generates the reference voltage by flowing a second current proportional to the first current through a series of the one of the bipolar transistor and the diode, and the resistor.

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4. A semiconductor integrated circuit, comprising:

a current generator circuit that generates 20 a first current substantially proportional to an absolute temperature; and

a voltage generator circuit that generates a reference voltage substantially independent of the absolute temperature using the first current

25 generated by said current generator circuit, wherein

said voltage generator circuit comprises:

a first element that generates a voltage that is substantially linealy reduced as the absolute temperature increases;

a resistance division circuit connected in parallel to said first element;

a second element connected to the parallel connection of said first element and said resistance division circuit, wherein said second element provides a second current proportional to the first current; and

a third element connected to a node between resistors of said resistance division circuit, wherein said third element provides a third current proportional to the first current.

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5. The semiconductor integrated circuit as 10 claimed in claim 4,

wherein

said first element is one of a bipolar transistor and a diode.

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 $\mbox{6. The semiconductor integrated circuit as} \\ \mbox{claimed in claim 4},$

20 wherein

said current generator circuit generates the first current determined by a size ratio of a MOS transistor, and by a resistor.

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- 7. A semiconductor integrated circuit, comprising:
- a first NMOS transistor that is provided with a voltage to a gate thereof, which voltage is generated by dividing a power supply voltage with resistors;
- a second NMOS transistor that is provided 35 with a reference voltage to a gate thereof;
 - a first PMOS transistor and a second PMOS transistor diode-connected to each other;

a third PMOS transistor, a gate of which is connected to a gate electrode of said first PMOS transistor;

a fourth PMOS transistor, a gate of which is connected to a gate electrode of said second PMOS transistor;

a third NMOS transistor connected as a diode;

a fourth NMOS transistor, a gate of which connected to the gate of said third NMOS transistor; and

a first resistor,
wherein

a source electrode of said first NMOS 15 transistor and a source electrode of said second NMOS transistor are connected together;

a drain of said first NMOS transistor and a drain of said first PMOS transistor are connected together;

a drain of said second NMOS transistor and a drain of said second PMOS transistor are connected together;

a drain of said third PMOS transistor and a drain of said third NMOS transistor are connected together;

a drain of said fourth PMOS transistor and a drain of said fourth NMOS transistor are connected together;

a first end of said first resistor is 30 connected to the power supply voltage;

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a second end of said first resistor is connected to the drain of said fourth PMOS transistor and to the drain of said fourth NMOS transistor; and

35 the semiconductor integrated circuit outputs a voltage of the second end of said first resistor for determining whether the power supply

voltage is lower than a predetermined voltage.

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\$8\$. The semiconductor integrated circuit as claimed in claim $\ensuremath{\text{7}}\xspace$,

wherein

the reference voltage is generated by the semiconductor integrated circuit as claimed in claim 2.

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- 9. A semiconductor integrated circuit, comprising:
 - a first pnp bipolar transistor;
 - a second pnp bipolar transistor;
- a first resistor connected in series to an emitter of said first pnp bipolar transistor;
 - a second resistor connected in series to an emitter of said second pnp bipolar transistor;
- a third resistor connected in series to an 25 end of said first resistor, resistance of said third resistor is equal to the resistance of the second resistor;

an operational amplifier that is provided with a voltage generated by level-shifting an emitter voltage of said second pnp bipolar transistor to a positive direction with said second resistor as a first input, and with a voltage generated by level-shifting a voltage at the end of said first resistor to a positive direction with

35 said third resistor as a second input,

wherein

said operational amplifier receives the

first input and the second input as a gate input of a differential pair of NMOS transistors, and is negatively fed back so that a voltage of the first input and a voltage of the second input are equalized.

10. The semiconductor integrated circuit as claimed in claim 9, further comprising:

a voltage generator circuit that generates a reference voltage substantially independent of an absolute temperature using a first current flowing through said first pnp bipolar transistor,

wherein

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said voltage generator circuit further
comprises:

a first element that generates a voltage 20 that is substantially linearly reduced as the absolute temperature increases;

a resistance division circuit connected in parallel to said first element;

a second element that provides a second 25 current proportional to the first current, said second element connected in parallel to the parallel connection of said first element and said resistance division circuit; and

a third element that provide a third

30 current proportional to the first current, the third
element connected to a node between resistors of
said resistance division circuit.